(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 381 479 A1**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: 90301018.9

(51) Int. Cl.[5] G09G 3/30

(22) Date of filing: 31.01.90

(30) Priority: 31.01.89 JP 23394/89

(43) Date of publication of application:
08.08.90 Bulletin 90/32

(84) Designated Contracting States:
DE GB

(71) Applicant: SHARP KABUSHIKI KAISHA
22-22 Nagaike-cho Abeno-ku
Osaka 545(JP)

(72) Inventor: Ogawa, Ikuo
1-2-50-501, Ukyo 2-chome
Nara-shi, Nara-ken(JP)
Inventor: Inohara, Akio
2-3-1105, Taishibashi 3-chome, Asahi-ku
Osaka-shi, Osaka-fu(JP)
Inventor: Ohba, Toshihiro
182-7, Kodonocho
Nara-shi, Nara-ken(JP)
Inventor: Kishishita, Hiroshi
12-5, Jingu 5-chome
Nara-shi, Nara-ken(JP)
Inventor: Uede, Hisashi
37 Honmachi 2-chome
Wakayama-shi, Wakayama-ken(JP)

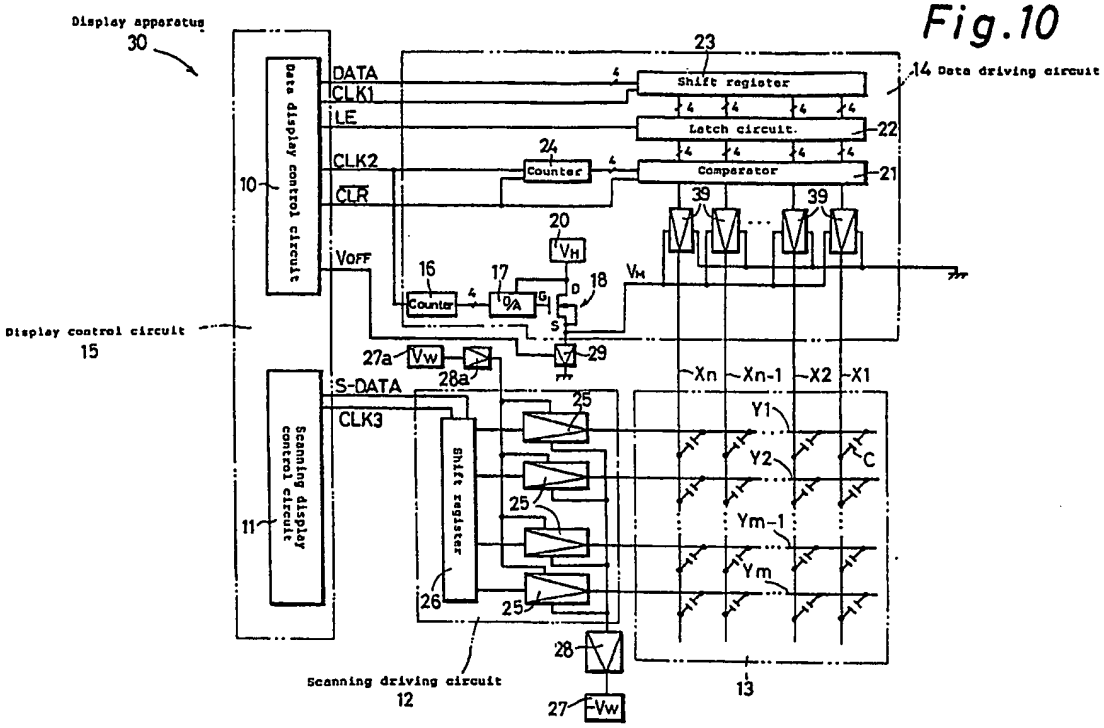
(74) Representative: Brown, Kenneth Richard et al
R.G.C. Jenkins & Co. 26 Caxton Street
London SW1H 0RJ(GB)

## (54) Method and apparatus for driving capacitive display device.

(57) This invention performs a gradation display in a capacitive display device (13) such as an EL display device by means of the pulse width control method (PWM method) in every pixel. In such case, it improves the changes of the driving voltage ($V_D$) in accordance with time and the reproducibility of the achievable voltage by setting the waveform of the driving voltage ($V_D$) applied between a pair of electrodes (X, Y) with an dielectric substance between them to change in steps corresponding to gradation display data (DATA). Thus, in display devices (30, 31) of the PAM method, the reproducibility of the waveforms of the voltage ($V_D$) applied to the pixels is improved, and the gradation display comes to be stable.

EP 0 381 479 A1

Fig.10


Display apparatus
30
Data display control circuit
10
DATA
CLK1
LE
CLK2
CLR
VOFF
Display control circuit
15
Scanning display control circuit
11
S-DATA
CLK3
Shift register
Scanning driving circuit
12
23
Shift register
14 Data driving circuit
Latch circuit
22
24
Counter
Comparator
21
39
20
VH
16
Counter
17
18
27a
Vw
28a
29
25
26
28
27
-Vw
Xn
Xn-1
X2
X1
Y1
Y2
C
Ym-1
Ym
13

# METHOD AND APPARATUS FOR DRIVING CAPACITIVE DISPLAY DEVICE

## 1. Field of the Invention

This invention relates to a method and apparatus for driving a capacitive display device such as an EL (electro luminescent) display device and a plasma display device.

## 2. Description of the Prior Art

For example, a double insulation type (or triple layer) thin film EL element is composed as follows.

As shown in Fig. 1, strips of transparent electrodes 2 made of $In_2O_3$ are formed parallel on a glass substrate 1, and an dielectric substance layer 3a of $Y_2O_3$, $Si_3N_4$, $TiO_2$, $Al_2O_3$ or the like, an EL substance layer 4 made of ZnS doped with an activator such as Mn, and a dielectric substance layer 3b of $Y_2O_3$, $Si_3N_4$, $TiO_2$, $Al_2O_3$ or the like are laminated thereon in a film thickness of 500 to 10.000 Å by thin film forming technique such as evaporation and sputtering method sequentially to form a triple layer structure, and strips of backside electrodes 5 made of Al (aluminum) are formed parallel thereon in an orthogonal direction to the transparent electrodes 2.

As the thin film EL element has the EL substance 4 held between the dielectric substance 3a and 3b placed between the electrodes 2 and 5, it may be regarded as a capacitive element from the viewpoint of equivalent circuit. This thin film EL element is driven, as apparently known from the brightness-voltage characteristic shown in Fig. 2, by applying a relatively high voltage of about 200V. This thin film EL element has such a characteristic that it emits light at high brightness by AC electric field as well as having a long durability.

In a display device using such a thin film EL element as its display panel, either the transparent electrodes 2 or the backside electrodes 5 are used as data side electrodes and the others as scanning side electrodes. A modulation voltage corresponding to the display data is applied to the data side electrodes. On the other hand, a writing voltage is applied line-sequentially to the scanning side electrodes.

By this drive, the superposing effect or canceling effect of the writing voltage and the modulating voltage occurs in the intersecting pixel part corresponding to each crossing position, and the driving voltage substantially applied to the pixel comes to be at the emission threshold or higher, or less than the emission threshold. Thus, each pixel is set in emission state or non-emission state, and a specified display is obtained.

Conventionally, in such a display apparatus, in the case that gradation display is performed by varying the brightness of each pixel in plural steps, pulse-width modulation method in which the width of pulse of the modulation voltage applied to the data side electrodes is varied corresponding to the gradation display data, and the amplitude modulation method in which the amplitude of the modulation voltage is varied corresponding to the gradation display data have been adopted.

In the pulse width modulation method, for the purpose of easy and constant gradation display, there is a method of using ramp voltage as the modulation voltage applied to the data side electrodes or the writing voltage applied to the scanning side electrodes. Meanwhile, "ramp voltage" is such voltage that the level of the voltage gradually increases or decreases as the time passes.

Figs. 3 and 4 show the circuit composition to generate the ramp voltage, respectively, and Figs. 5 and 6 are timing charts showing the operation of the circuits in Fig. 3 and Fig. 4, respectively.

In a ramp voltage generating circuit shown in Fig. 3, a constant current circuit 6 is a circuit that supplies constant electric current receiving a starting signal $V_{ON}$ of the ramp voltage from outside, and it is connected to one of the terminals of a capacitor 7 as well as the power source HVCC. The other terminal of the capacitor 7 is grounded. A converter 8 is a circuit that outputs the ramp voltage $V_R$ corresponding to the charging voltage of capacitor 7 as it receives the charging voltage, and it is connected to the connecting point A of the constant current circuit 6 and the capacitor 7 as well as the power source HVCC. In addition, between the connecting point A and the ground, a switch circuit 9 that comes to be in ON state as it receives the terminating signal $V_{OFF}$ of the ramp voltage from outside is connected.

In this ramp voltage generating circuit, when the starting signal $V_{ON}$ of the ramp voltage shown in Fig. 5(1) is applied, the constant current circuit 6 comes to be in ON state a constant current starts to flow in the capacitor 7 through the constant current circuit 6 from the power source HVCC, and the charging voltage of the capacitor 7 increases with a specified gradient as the time passes. When the specified time has passed and the starting signal $V_{ON}$ of the ramp voltage is discontinued, the constant current circuit 6 comes to be in OFF state, and the charging of the capacitor 7 is terminated. Succeedingly, when the terminating signal $V_{OFF}$ of the ramp voltage shown in Fig. 5(2) is applied, the switch circuit of become to conductive state, and the capacitor 7 starts discharging through the

switch circuit 9, and the charging voltage of the capacitor 7 remarkably decreases. From the converter 8, the ramp voltage $V_R$ corresponding to the changes in the charging voltage of the capacitor 7 therein, as shown in Fig. 5(3), is output.

In a ramp voltage generating circuit shown in Fig. 4, the constant current circuit 6 and the switch circuit 9 in Fig. 3 are replaced. When the starting signal $V_{ON}$ of the ramp voltage shown in Fig. 6(1) is applied, the switch circuit 9 comes to be in ON state, the capacitor 7 is charged through this switch circuit 9 from the power source HVCC, and the charging voltage of the capacitor 7 rapidly increases to the voltage of the power source HVCC.

After the starting signal $V_{ON}$ of the ramp voltage is discontinued and the switch circuit 9 is cut, when the terminating signal $V_{OFF}$ of the ramp voltage shown in Fig. 6(2) is applied, the constant current circuit 6 comes to be in ON action, a constant electric current starts to be supplied from the capacitor 7 through the constant current circuit 6 to the ground, and the charging voltage of the capacitor 7 rapidly decreaes with a specified gradient as the time passes. From the converter 8, the ramp voltage $V_R$ shown in Fig. 6(3) which corresponds to the changes in the charging voltage of the capacitor 7 therein is output.

However, in the case of obtaining the ramp voltage $V_R$ by charging and discharging of the capacitor 7 as mentioned herein above, as the gradient of the ramp voltage $V_R$ , for example, is determined by the resistance value of the constant current circuit 6 and the capacity of the capacitor 7, the reproducibility of the waveform of the obtained ramp voltage $V_R$ is poor due to the differences in characteristics of circuit elements such as transistors, resistors and capacitors composing the ramp voltage generating circuit. Moreover, due to the differences in timings for applying the starting signal $V_{ON}$ of the ramp voltage and the terminating signal $V_{OFF}$ of the ramp voltage, the achievable voltage of the ramp voltage $V_R$ varies as well, which is another problem.

## SUMMARY OF THE INVENTION

It is hence a primary object of the invention to present a method and apparatus for driving a display device which enables a superior reproducibility of the voltage waveform applied to pixels and a stable gradation display in driving a capacitive display device for the displaying purpose.

These object and other object have been attained by the driving method for a display device that display by applying a pulse signal between the electrodes of the display device composed of dielectric substances placed between a pair of electrodes, in which the level exceeding the threshold to start displaying operation changes as the time passes.

In the driving method of a display device of the invention, the changes in the level exceeding the threshold in the pulse signal is preferably in steps, and the average time-course changing rate is selected to follow a function priorly set in terms of the time.

This invention presents a driving method for a display device composed of dielectric substances placed between plural scanning side electrodes and plural data side electrodes aligned in mutually crossing directions, wherein a writing voltage is applied in line-sequentially to the scanning electrodes, a modulation voltage that changes in pulse width corresponding to the gradation display data is applied to the data electrodes, and between the scanning electrodes and the data electrodes, a driving voltage of which level exceeding the threshold for starting the displaying operation changes in steps corresponding to the gradation display data is applied.

This invention presents a driving method for a display device which has dielectric substances placed between plural scanning electrodes and plural data electrodes aligned in mutually crossing directions and performs a gradation display by applying a modulation voltage that changes in pulse width corresponding to the gradation display data to the data side electrodes as well as applying a writing voltage is line-sequentially to the scanning electrodes, wherein a voltage having such a waveform that gradually increases its level in steps is used as the modulation voltage applied to the data side electrodes or the writing voltage applied to the scanning electrodes.

In a preferred embodiment, in a driving method of a display device composed of dielectric substances placed between plural scanning side electrodes and plural data side electrodes aligned in mutually crossing directions, a writing voltage is applied in line-sequentially to the scanning side electrodes, and a modulation voltage that changes in pulse width corresponding to the gradation display data and that changes its level in steps is applied to the data side electrodes.

In a preferred embodiment, in a driving method of a display device composed of dielectric substances placed between plural scanning electrodes and plural data electrodes aligned in mutually crossing directions, a writing voltage that changes its level in steps is applied to the scanning side electrodes, and a modulation voltage that changes in pulse width corresponding to the gradation display data is applied to the data side electrodes.

This invention presents a driving apparatus for a display device comprising a display element

composed of dielectric substances placed between plural scanning electrodes and plural data electrodes aligned in mutually crossing directions, a driving circuit in the scanning side which applies a writing voltage in line-sequentially to the scanning electrodes, a driving circuit in the data side which applies a modulation voltage changing in pulse width corresponding to the gradation display data to the data electrodes, and a staircase wave generating circuit which is formed at least in one of the driving circuits in the scanning side and the driving circuits in the data side and generates a staircase wave to change the waveform of the driving voltage applied between the scanning side electrodes and the data side electrodes at the level exceeding the threshold for performing displaying operation.

In a driving apparatus for a display device of the invention, the driving voltage is chosen to follow a function that the average time-course changing rate of the level is priorly set in terms of the time.

In a preferred embodiment, the staircase wave generating circuit comprises a first counter which performs calculations based on the data showing the gradation of plural bits input in every scanning period and the clock signals, a digital-to-analogue (D-A) converter which converts the output calculation values of the first counter to analogue values, and a driving circuit which forms a modulation voltage waveform supplied to the data side electrodes in correspondence with the output of the D-A converter.

In a preferred embodiment, the driving circuit applies a modulation voltage which is supplied to the display element together with a writing voltage and is at the threshold level or higher voltage for starting the displaying operation or less than the threshold level.

In a preferred embodiment, between the first counter and the D-A converter, a conversion circuit is connected, which converts the time-course changing rate of the driving voltage applied between the scanning side electrodes and the data side electrodes corresponding to the output calculation value of the first counter.

In a preferred embodiment, the conversion circuit has a memory and outputs the data priorly stored in to the D-A converter corresponding to the output calculation value of the first counter.

In a preferred embodiment, the staircase wave generating circuits is formed in the data side driving circuit, and such embodiment comprises a circuit which generates data showing the gradation of plural bits corresponding to each data side electrode in every scanning period that a writing voltage is applied in line- sequentially to each scanning side electrode, second counter which performs calculations based on the clock signals in every scanning period of the scanning side electrodes, a comparator which compares the output gradation display data and the output calculation values of the second counter to determine the pulse width of the modulation voltage applied to each data side electrode, and a modulation voltage forming circuit which forms and supplies the modulation voltage waveform in steps to each data side electrode in correspondence with the output of the comparator and the output of the staircase wave generating circuit.

In a preferred embodiment, the scanning side driving circuit includes the staircase wave generating circuit, and applies a superposed voltage of the writing voltage and the staircase wave voltage to each scanning side electrode in a line-sequentially in each scanning period.

According to the invention, as a voltage having a waveform of levels changing in steps is applied to the data side electrodes or the scanning side electrodes as a modulation voltage or a writing voltage, the reproducibility of the waveforms of a modulation voltage or a writing voltage is not deteriorated due to the differences in characteristics of circuit elements. In addition, the differences in starting timings and terminating timings of the modulation voltage or the writing voltage do not affect the achievable voltage, the reproducibility of voltage waveforms applied to pixels is improved, and the gradation display comes to be stable.

## BRIEF DESCRIPTION OF THE DRAWINGS

These objects and other objects, characteristics and advantages of the invention will be better understood through a detailed description and drawings herein below.

Fig. 1 is a partially cut-away perspective view of a thin film EL element.

Fig. 2 is a diagram showing a relative brightness-applied voltage characteristic of a thin film EL element.

Fig. 3 is a block diagram schematically showing a composition example of a conventional ramp voltage generating circuit.

Fig. 4 is a block diagram schematically showing a composition example of the other conventional ramp voltage generating circuit.

Fig. 5 is a timing chart showing the operation of the ramp voltage generating circuit in Fig. 3.

Fig. 6 is a timing chart showing the operation of the ramp voltage generating circuit in Fig. 4.

Fig. 7 is a block diagram showing the basic composition of a display apparatus.

Fig. 8 is a block diagram showing the basic composition of a staircase wave generating circuit of one of the embodiments of the invention.

Fig. 9 is a timing chart showing the operation of the staircase wave generating circuit in Fig. 8.

Fig. 10 is a block diagram showing the composition of a display apparatus 30 of one of the embodiments of the invention.

Fig. 11 is a timing chart showing the operation of setting a gradation width of a display apparatus 30.

Fig. 12 is a waveform diagram showing voltages applied to a display apparatus 30 in gradation display drive.

Fig. 13 is a wave form diagram explaining the current flowing in a light-emitting layer.

Fig. 14 is a block diagram showing the composition of a display apparatus 31 of the other embodiment of the invention.

Fig. 15 is a waveform diagram showing voltages applied to a display apparatus 31 in gradation display drive.

Fig. 16 is a block diagram showing the other composition example of a staircase wave generating circuit.

Fig. 17 is a timing chart showing the operation of a staircase wave generating circuit in Fig. 16.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refering now to the drawings, preferred embodiments of the invention are described in detail below.

Fig. 7 is a block diagram showing the basic composition of a display apparatus. Scanning side electrodes Y of a display part 13 are connected to a scanning side driving circuit 12. On the other hand, data side electrodes X of the display part 13 are connected to a data side driving circuit 14. To the scanning side driving circuit 12 and the data side driving circuit 14, a display control circuit 15 is connected, which controls the operations of the circuits 12 and 14.

The data side driving circuit 14 has a function that can set the pulse width of modulation voltage applied to each data side electrode X according to the gradation display data supplied from a display control circuit 15. The scanning side driving circuit 12 has a function of applying a writing voltage to the scanning side electrodes Y in a line-sequentially.

Fig. 8 is a block diagram showing the basic composition of a staircase wave generating circuit generating a staircase wave voltage $V_S$ . A counter 16 is a circuit to count the clock signal $\phi$ for gradation supplied from the display control circuit 15, and has a function to output, for example, the counted value as binary cords "Q3, Q2, Q1, Q0" of four bits.

In the succeeding stage of the counter 16, a digital- to-analogue converter (D-A converter) 17 converting the outputs "Q3, Q2, Q1, Q0" of four bits into analogue signals, that is, voltages $V_A$ , is connected, and a power source HVCC is supplied to this D-A converter 17. The output $V_A$ from the D-A converter 17 is converted to a staircase wave voltage $V_S$ by a converter 18 supplied with electricity by the power source HVCC.

The converter 18 is realized by a MOS transistor of P channel, for example, as shown in Fig. 8, and the output terminal of the D-A converter 17 is connected to the gate G of this transistor, the drain D is supplied with the power source HVCC, and the source S is connected to the output stage of the aforementioned data side driving circuit 14 or the scanning side driving circuit 12 (see Fig. 7).

Fig. 9 is a timing chart showing the operation of the staircase wave generating circuit. In the case that the staircase voltage $V_S$ is supplied to the output stage of the data side driving circuit 14 shown in Fig. 7, when the application of the writing voltage - $V_W$ ( = -$V_{th}$, where $V_{th}$ is a voltage of emission threshold) is started to one scanning side electrode Y chosen by the scanning side driving circuit 12, the counter 16 of the staircase wave generation circuit shown in Fig. 8 simultaneously starts counting the clock signals $\phi$ (see Fig. 9(1)) for gradation. Thereby, the clock signals $\phi$ for gradation are devided into the output waveforms Q0 to Q3 shown in Fig. 9(2). The outputs "Q3, Q2, Q1, Q0" are the counted values of the clock signals $\phi$ for gradation expressed by binary cords of four bits, and from the D-A converter 17 to which the four-bit data is input a voltage $V_A$ in a level corresponding to the input data is output.

In other words, as shown in Fig. 9(3), the output voltage $V_A$ of the D-A converter 17 has such a waveform in steps that it increases one step every time when the counter 16 counts a clock signal $\phi$ for gradation. Therefore, a voltage $V_S$ output from the source S of the P-channel MOS transistor 18 of the succeeding stage which receives the output voltage $V_A$ as a gate voltage changes according to the voltage $V_A$ as well, and thereby, the output voltage $V_S$ can be obtained as a similar staircase wave to the voltage $V_A$ in the case of neglecting the reduction in voltage between the gate and the source of the transistor 18. The P-channel MOS transistor 18 should have a sufficient capacity for supplying electricity, and the output voltage $V_S$ of the source should not change through a load of the succeeding stage.

In the case that the staircase wave voltage $V_S$ obtained in such manner is supplied to the output stage of the data side driving circuit 14, it is applied to the data side electrodes X as a modula-

tion voltage $V_M$. On the other hand, in the case that it is applied to the output stage of the scanning side driving circuit 12, for example, the staircase wave voltage $V_S$ is superposed by the writing voltage - $V_W$ and is applied to the scanning side electrodes Y.

Theoretically, by forming the counter 16 and the other circuits as power source circuit of each data side driving circuit 14 and setting the gradation display data supplied by the display control circuit 15 (see Fig. 7) in correspondence with each data side electrode X as a load value of the counter 16, when the counting value reaches the load value of the gradation display data, the counter 16 is cleared, and then, the staircase wave voltage $V_S$ is lowered as well. Thus, the staircase wave voltage $V_S$ with a pulse width corresponding to the gradation display data is applied to the data side electrodes X from the data side driving circuit 14 as a modulation voltage $V_M$.

Fig. 10 is a block diagram showing the electrical composition of a display apparatus 30 of the embodiments of the invention. In the embodiment, the staircase wave generating circuit is composed as a part of the data side driving circuit 14, and the back edge of the staircase wave voltage $V_S$ obtained is set by cutting off according to the gradation display data DATA. The display device 30 is, for example, an EL display device, and the display part 13 forming the EL display panel is composed of, for example, thin film EL (electroluminescent) elements of double insulated type (see Fig. 1)

Meanwhile, each pixel in the display part 13 is expressed equivalently in a capacitor C. Plural data side electrodes X1, X2, ... Xn-1, Xn (shown by a reference sign X in general) are connected to the data side driving circuit 14. Plural scanning side electrodes Y1, Y2, ... Ym-1, Ym (shown by a reference sign Y in general) aligned in a direction of mutually crossing with the data side electrodes X1 to Xn are connected to the scanning side driving circuit 12.

In the scanning side driving circuit 12, an output port 25 is connected individually to the scanning side electrodes Y1 to Ym, and through the output port 25, a writing voltage - $V_W$ is selectively applied to the scanning side electrodes Y1 to Ym from a power source circuit 27 via a driver 28. A shift resister 26 is connected to each output port 25. Synchronized with the clock signal CKL3 from the scanning side display control circuit 11, a scanning data S-DAT which designates the scanning side electrodes Y1 to Ym line-sequentially is transmitted to the shift resister 26, and thereby, each output port 25 comes to be in ON action line-sequentially according to the scanning side electrodes Y1 to Ym.

On the other hand, in the data side driving circuit 14, an output port 39 is connected individually to the data side electrodes X1 to Xn, and through the output port 39, a modulation voltage $V_M$ is applied to the data side electrodes X1 to Xn from a power source circuit 20 via a transistor 18. In addition, according to a setting state of the output port 39, the data side electrodes X1 to Xn are clamped to the ground.

These output ports 39 are connected to a comparator 21. This comparator 21 is connected to a shift register 23 through a latch circuit 22. The shift register 23 shifts the gradation display data DATA input in synchronization with the clock signal CLK1 from the data side display control circuit 10, and transmits, for example, a gradation display data DATA expressed by pallarel data of four bits in correspondence with each of the data side electrodes X1 to Xn. After being transmitted by the shift register 23, the gradation display data DATA is latched in the latch circuit 22 according to the latch signal LE from the data side display control circuit 10 and supplied to the comparator 21.

The comparator 21 compares the pallarel data of four bits supplied from the counter 24 with the gradation display data DATA supplied from the latch circuit 22, and functions to determine the pulse width of the modulation voltage $V_M$ corresponding to the gradation display data DATA.

Fig. 11 is a timing chart showing the basic operation of the EL display apparatus 30 shown in Fig. 10. To the shift register 23 of the data side driving circuit 14, the gradation display data DATA is transmitted in a shape of a binary cord of four bits in synchronization with the clock signal CLK1. The gradation display data DATA in four bits is temporarily held in the latch circuit 22. In such state, in the case that a clear signal $\overline{CLR}$ remaining input in the comparator 21 and the counter 24 is released at a time t1 as shown in Fig. 11(1), the data electrode X corresponding to data "0" out of the gradation display data held in the latch circuit 22 is clamped to the ground, and the data side electrodes X corresponding to the other data are all drawn to the modulation voltage $V_M$.

For example, such a case is supposed that gradation display data "0", "2", "4", "7" are supplied to the output ports 39 corresponding to the data side electrodes X1, X2, Xn-1, Xn of the data side driving circuit 14. In this case, the output port 39 of the data side electrode X1 is clamped to the ground simultaneously with the release of the clear signal $\overline{CLR}$, and the wave form comes to have a shape as shown in Fig. 11(3). In other words, the gradation width is set at zero.

In the output port 39 of the data side electrode X2, the counted value of the clock signal CLK2 (see Fig. 11(2)) counted by the counter 24 is compared with the gradation display data "2" by the

comparator 21, and at a timing (time t2) when the counted value comes to be "2", it is clamped to the ground and a gradation width T2 of a waveform shown in Fig. 11(4) is set.

Similarly, the output port 39 of the data side electrodes Xn-1 is clamped to the ground at a timing (time t3) when the counted value of the counter 24 comes to be "4", and a gradation width T4 of a waveform shown in Fig. 11(5) is set.

In regard to the output port 39 of the data side electrode Xn, it is clamped to the ground as well at the timing (time t4) when the counted value of the counter 24 comes to be "7", and a gradation width T7 of a waveform shown in Fig. 11(6) is set.

Therefore, the modulation voltage $V_M$ with a pulse width equivalent to the gradation display data "0", "2", "4", "7" are applied to each of the data side electrodes X1, X2, Xn-1 and Xn.

On the other hand, in the scanning side driving circuit 12, while the clear signal $\overline{CLR}$ is released in the data side driving circuit 14, only one of all output ports 25 comes to be in ON action, and the writing voltage - $V_W$ is applied only to one scanning side electrode Y selected in correspondence with this.

By a succession of the aforementioned actions in accordance to the line sequence of the scanning side electrodes Y, pixels positioned on each scanning side electrode Y emit a light at a brightness corresponding to the gradation display data DATA, or stops the emission of light, and as a whole, an image with a gradation in brightness is displayed.

A driving voltage $V_D$ applied to the pixel corresponding to the crossing position of the scanning side electrode Y to which the writing voltage - $V_W$ is applied and the data side electrode X to which the modulation voltage $V_M$ is applied comes to have a waveform shown in Fig. 12(3) based on the scanning side electrode Y.

In the waveform of the driving voltage $V_D$, the shaped area exceeding the emission threshold voltage $V_{th}$ corresponds to the part where the modulation voltage $V_M$ in steps shown in Fig. 12(1) superposes on the writing voltage - $V_W$ (= $-V_{th}$), and thus, the pixels emit lights at a brightness according to the gradation display data. The modulation voltage $V_M$ has a pulse width T according to the gradation display data DATA, and as shown in Fig. 12(1), it can be changed up to the highest level VH allowed by the output voltage from the power source circuit 20 in Fig. 10.

As apparently known from the wave form of the driving voltage $V_D$ shown in Fig. 12(3), in the case of such driving method, the modulation voltage $V_M$ increases in steps synchronizing with the clock signal CLK2 for gradation, and as in the period of one step, the timing for cutting off the modulation voltage $V_M$ is also determined by the gradation width T determined in accordance to the counter 24 counting in synchronization with the clock signal CLK2, achievable voltages of the driving voltage $V_D$ never vary. Moreover, since a ramp wave form by charging and discharging of a capacitor is not used as the modulation voltage $V_M$, differences in levels of the modulation voltage $V_M$ (variation of $dV_D/dt$ of a ramp waveform) caused by the differences in characteristics of the elements composing the circuit do not occur as in the case of a ramp waveform, the modulation voltage $V_M$ comes to be stable, and therefore, a stable gradation display can be realized.

In the case that the driving voltage $V_D$ applied to the corresponding pixels has such a waveform as shown by a solid line in Fig. 13(1) , the waveform of the electric current of the power source, as shown in Fig. 13(2), comes to have a longer feed time after the driving voltage $V_D$ comes to be at the emission threshold voltage $V_{th}$ or higher voltages. Moreover, the driving voltage $V_D$ is not a square wave, and as it comes to have such a waveform that the writing voltage $V_W$ of a square wave and a modulation voltage $V_M$ having waveform in steps are superposed, the electric current of the power source smoothly reduces without being a peak current.

Such tendency is directly reflected in the electric current flowing in the emission layer of the pixel, and as shown in Fig. 13(3), the waveform of the electric current is controlled to have a lower peak value and smoothly reduces to have a waveform with a longer feed time.

On the other hand, by setting the pulse width of the modulation voltage $V_M$ in steps at a shorter width dividing it into some steps as shown by a single-dotted broken line 21 in Fig. 13(1), the feed time of the electric current flowing in the emission layer of the pixel shown in Fig. 13(3) can be also shortened.

Generally, the brightness level of a light emitted from a emission layer such as an EL substance is proportional to the level of the electric current running in the emission layer and the length of the feed time. Therefore, in this case, since the feed time of the electric current running in the emission layer of pixels is longer than the conventional case, the range of changeably setting the pulse width of the modulation voltage $V_M$, that is, the effective motion range shown with a reference sign t in Fig. 13 (1) is wider, and the gradation display in multiple stages corresponding to the number of output bits of the counter 16 can be performed easily and precisely.

In addition, as the peak value of the electric current running in the emission layer of pixels is controled to be at a low value, the current value at the brightness in each gradation stage comes to be

low, and the gradation in each stage can be stably displayed without any remarkable changes in brightness due to errors in pulse widths of the modulation voltage $V_M$.

Fig. 14 is a block diagram showing a display apparatus 31, where in the staircase wave generating circuit shown in Fig. 8 is composed as a part of the scanning side driving circuit 12, and the staircase wave voltage - $V_S$ obtained is used in superposition with the writing voltage - $V_W$ (= $-V_{th}$). Fig. 15 is a waveform diagram showing the voltages applied in driving the gradation display.

In the data side driving circuit 14 of the display apparatus 31 shown in Fig. 14, a modulation voltage $V_M$ is supplied to the output port 39 connected individually in correspondence with the data side electrodes X1 to Xn from the power source circuit 32 through the modulation driver 33.

On their other hand, in the scanning side driving circuit 12, a voltage - ($V_{th}$ - $V_H$) is supplied to the output port 25 connected individually in correspondence with the scanning side electrodes Y1 to Ym from the power source circuit 38 through the writing driver 37, and a staircase wave voltage - $V_S$ from the staircase wave generating circuit is superposed on the voltage - ($V_{th}$ - $V_H$ to make a voltage - $V_W$.

In the staircase wave generating circuit, the counter 16 counts based on the clock signal CLK2 from the data side display control circuit 10, and supplies a binary cord output of four bits to the D-A converter 17. To the D-A converter 17, a voltage - $V_H$ is supplied from the power source circuit 34, and the digital signal output from the counter 16 is converted into a staircase wave voltage $V_A$ and is supplied to the conveter 18. For example, a voltage - $V_H$ from the power source circuit 34 is also supplied to the converter 18 composed by a MOS transistor of P channels and the like, and a staircase wave voltage - $V_S$ corresponding to the output voltage of the D-A converter 17 is supplied to each output port 25.

At the connection 40 of the D-A converter 17 and the converter 18, a power source circuit 34 is connected through a capacitor 35 and is grounded through a switch circuit 36. In the switch circuit 36, a control signal $V_{OFF}$ is supplied from the scanning side control circuit 11.

Therefore, the converter 18 receives the charging voltage (the electric potential of the connection 40 of the D-A converter 17 and the capacitor 35) of the capacitor 35 and outputs a voltage - VS corresponding to that electric potential. The switch circuit 36 comes to be in ON state by the control signal $V_{OFF}$ supplied from the scanning side control circuit 11, the connection 40 is lowered to the ground level, and the output voltage - $V_S$ from the converter 18 to the output port 25 is cut off.

In such case, the modulation voltage $V_M$ is applied to the data side electrode X (Fig. 14) as a short wave with a pulse width corresponding to the gradation display data as shown in Fig. 15(1). On the other hand,k the writing voltage -$V_W$ is applied, as shown in Fig. 15(2), in such a waveform that a negative staircase wave voltage - $V_S$ is superposed on a specific voltage of - ($V_{th}$ - $V_H$) (where $V_H$ is the highest level of the staircase wave voltage $V_S$) to the scanning side electrode Y (Fig. 14). Therefore, the wave form based on the scanning side electrode Y of the driving voltage $V_D$ applied to the corresponding pixel comes to have such a waveform as shown in Fig. 15(3).

In the waveform of the driving voltage $V_D$ , the voltage area at the emission threshold voltage $V_{th}$ or higher voltages is equivalent to the superposing part of the staircase wave voltage $V_S$. In such case, though in the voltage area at the emission threshold voltage $V_{th}$ or lower voltages, a waveform different from the wave form shown in Fig. 12(3) is generated in some parts, as in the voltage area at the emission threshold voltage $V_{th}$ or higher voltages contributing directly to the emission of lights from the pixels, the waveforms are same as shown in Fig. 12(3), no problem is caused.

Fig. 16 is a block diagram showing the basic composition of the other staircase wave generating circuit having a different composition from that of the staircase wave generating circuit shown in Fig. 8. In the circuit shown in Fig. 16, a memory 19 is placed and connected between the counter 16 and the D-A converter 17 of the circuit shown in Fig. 8, and the other composition is same as in Fig. 8.

The memory 19 realized by a read-only-memory (ROM), a read-write-memory (RWM) and the like receives the outputs "Q3, Q2, Q1, Q0" of the counter 16 as address designating signals "A3, A2, A1, A0", and functions to send data "D3, D2, D1, D0" of four bits to the D-A converter 17 in the succeeding stage, and in each storing area, data is priorly stored in order to output the desired staircase wave voltage $V_A$ corresponding to the outputs "Q3, Q2, Q1, Q0" of the counter 16.

Fig. 17 is a timing chart showing the operation of the staircase wave generating circuit shown in Fig. 16. The clock signal for gradation shown in Fig. 17(1) and the output waveform of the counter 16 shown in Fig. 17(2) are same as in the case of Fig. 9.

In such case, as the outputs "Q3, Q2, Q1, Q0" of the counter 16 are entered into the D-A converter 17 by the memory 19 in such a form that they are converted to different data "D3, D2, D1, D0" corresponding to the outputs, from the D-A converter 17, for example, as shown in Fig. 17(3), a staircase wave voltage $V_A$ different in the average changing rate of increase of the voltage level from

the case shown in Fig. 9(3) can be obtained. In other words, in this staircase wave generating circuit, by placing the memory 19, a desired staircase wave voltage $V_A$ can be generated. Such composition of placing the memory 19 is effective especially in such case that the brightness level of emitted lights is adjusted to be equally divided in consideration of sight characteristics of a human eye for the purpose of gradation display.

In the embodiments described above, such case has been explained that the outputs of the counter 16 or the memory 19 are a number of bit, for example, four bits corresponding to that of the gradation display data DATA to output the staircase wave voltage $V_A$ of the 16 steps from the D-A converter 17, but the bit number is not thus limited and may be set at a desirable number according to the gradation degree of the gradation display.

In addition, in regard to the D-A converter 17, such case has been explained that the output voltage, that is the staircase wave voltage $V_A$ increases as the counted value of the counter 16 increases, but reversely, the D-A converter may have such a function that the staircase wave $V_A$ output from the D-A converter decreases as the counted value increases.

In the embodiment, the case of the writing voltage $V_W$ of negative polarity is explained, this invention is applicable to the case of the writing voltage $V_W$ of positive polarity. In other words, in case of Fig. 10 as the writing voltage $V_W$ of positive polarity from the power source 27a is supplied to the output port 25 through the writing driven 28a, the writing voltage $V_W$ is applied to scanning side electrode Y1 - Ym line-sequentially in according to each output port 25 which achieve ON action by shiftregister 26.

Moreover, although in the foregoing embodiments, the invention has been explained in such case that the EL display device is driven, it is not limited to this but is also applicable in driving a plasma display, a liquid crystal display device and other capacitive display devices.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and the range of equivalency of the claims are therefore intended to be embraced therein.

There are described above novel features which the skilled man will appreciate give rise to advantages. These are each independent aspects of the invention to be covered by the present application, irrespective of whether or not they are included within the scope of the following claims.

## Claims

1. In a method for driving display devices (30, 31) which display by applying a pulse signal ($V_D$) between the electrodes (X, Y) of a display apparatus composed by placing an dielectric substance between a pair of electrodes (X, Y) , the method comprising the action, that the pulse signal ($V_D$) changes its level of exceeding the threshold ($V_{th}$) where the display action starts as the time passes.

2. A method for driving display devices (30, 31) according to claim 1, wherein changes in level of exceeding the threshold ($V_{th}$) in the pulse signal ($V_D$) are in steps, and the average time-course changing rate is selected so as to follow a function priorly specified in terms of the time.

3. In a method for driving a display device (13) composed by placing an dielectric substance between plural scanning side electrodes (Y1 to Ym) and plural data side electrodes (X1 to Xn) aligned in mutually crossing directions, the method comprising the action that a writing voltage ($V_M$) is applied line-sequentially to the scanning side electrodes (Y1 to Ym) , a modulation voltage ($V_M$) changing in pulse width (T) in correspondence with a gradation display data (DATA) is applied to the data side electrodes (X1 to Xn), and between the scanning side electrodes (Y1 to Ym) and the data side electrodes (X1 to Xn) , a driving voltage ($V_D$) of which level of exceeding the threshold ($V_{th}$) for starting the display action changes in steps in correspondence with the gradation display data (DATA).

4. In a method for driving display devices (30, 31) in which an dielectric substance is placed between plural scanning side electrodes (Y1 to Ym) and plural data side electrodes (X1 to Xn) aligned in mutually crossing directions, a modulation voltage ($V_M$) changing in the pulse width (T) in correspondence with a gradation display data (DATA) is applied to the data side electrodes (X1 to Xn) and a writing voltage ($V_W$) is applied in a linear sequence to the scanning side electrodes (Y1 to Ym) in order to perform a gradation display, the method comprising the action;
that a voltage having waveform with its level gradually changing in steps is used as the modulation voltage ($V_M$) applied to the data side electrodes (X1 to Xn), or the writing voltage ($V_M$) applied to the scanning side electrodes (Y1 to Ym).

5. In a method for driving display devices (30, 31) composed by placing an dielectric substance between plural scanning side electrodes (Y1 to Ym) and plural data side electrodes (X1 to Xn) aligned

in mutually crossing directions, the method comprising the action;
that a writing voltage ($V_W$) is applied line-sequentially to the scanning side electrodes (Y1 to Ym) , and a modulation voltage ($V_M$) changing its pulse width (T) in correspondence with a gradation display data (DATA) and its level in steps is applied to the data side electrodes (X1 to Xn).

6. In a method for driving display devices (30, 31) composed by placing an dielectric substance between plural scanning side electrodes (Y1 to Ym) and plural data side electrodes (X1 to Xn) aligned in mutually crossing directions, the method comprising the action;
that a writing voltage ($V_W$) changing its level in steps corresponding with a gradation display data (DATA) is applied to the scanning side electrodes (Y1 to Ym), and a modulation voltage ($V_M$) changing its pulse width (T) in correspondence with the gradation display data (DATA) is applied to the data side electrodes (X1 to Xn)

7. An apparatus for driving display devices (30 and 31) comprising:
a display element (13) composed by placing an dielectric substance between plural scanning side electrodes (Y1 to Ym) and plural data side electrodes (X1 to Xn) aligned in mutually crossing directions,
a scanning side driving circuit (12) applying a writing voltage ($V_W$) in a linear sequence to the scanning side electrodes (Y1 to Ym),
a data side driving circuit (14) applying a modulation voltage ($V_M$ ) which changes its pulse width (T) in correspondence with a gradation display data (DATA) to the data side electrodes (X1 to Xn),
a staircase wave generating circuits (16 to 19) formed at least in one of the scanning side driving circuit (12) and the data side driving circuit (14) and generating a staircase wave in order to change the wave form of a driving voltage ($V_D$) applied between the scanning side electrodes (Y1 to Ym) and the data side electrodes (X1 to Xn) at a level of exceeding the threshold ($V_{th}$) for starting display action in steps in correspondence with the gradation display data (DATA).

8. An apparatus for driving display devices (30 and 31) according to claim 7, wherein the driving voltage ($V_D$) is selected in such a manner that the average time-course changing rate in its level follows a function priorly specified in terms of the time.

9. An apparatus for driving display devices (30 and 31) according to claim 7, wherein the staircase wave generating circuits (16 to 19) comprise a first counter (16) which calculates based on data (DATA) expressing the gradation of plural bits entered in each scanning period and a clock signal (CLK2), a digital-to-analogue converter (17) which converts the output calculated value of the first counter (16) into an analogue value, and a driving circuit (18) which forms the waveform of a modulation voltage ($V_M$) supplied to the data side electrodes (X1 to Xn) responding to the output of the D-A converter (17).

10. An apparatus for driving display devices (30, 31) according to claim 9, wherein the driving circuit (18) applies a modulation voltage ($V_M$) which is supplied to a display element (13) together with a writing voltage ($V_W$) and is at the threshold ($V_{th}$) level or higher, or less than the threshold ($V_{th}$) level to the data side electrodes (X1 to Xn).

11. An apparatus for driving display devices (30, 31) according to claim 9, wherein a conversion circuit (19) which converts the time-course changing rate of the driving voltage ($V_D$ ) applied between the scanning side electrodes (Y1 to Ym) and the data side electrodes (X1 to Xn) in response to the output calculated value of the first counter (16) is placed between the first counter (16) and the D-A converter (17).

12. An apparatus for driving display devices (30, 31) according to claim 11, wherein the conversion circuit (19) has a memory function, and data (D0 to D3) priorly stored are sent out to the D-A converter (17) in response to the output calculated value of the first counter (16).

13. An apparatus for driving display devices (30 31) according to claim 7, comprising further:
staircase wave generating circuits (16 to 19) formed in the data side driving circuit (14),
circuits (10, 22, 23) generating data (DATA) which expresses the gradation of plural bits in correspondence with each of the data side electrodes (X1 to Xn) in every scanning period in which a writing voltage ($V_W$) is applied in a linear sequence to each of the scanning side electrodes (Y1 to Ym),
second counter (24) performing a calculation in each scanning period of the scanning side electrodes (Y1 to Ym) based on the clock signal (CLK2),
a comparator (21) which compares the output of the gradation display data (DATA) with the output of the calculated data of the second counter (24) to determine the pulse width (T) of a modulation voltage applied to each of the data side electrodes (X1 to Xn)
and a modulation voltage forming circuit (39) forming and supplying a waveform of the modulation voltage ($V_M$ ) in steps to the data side electrodes (X1 to Xn) in response to the output of the comparator (21) and the output of the staircase wave generating circuits (16 to 19).

14. An apparatus for driving display devices (30, 31) according to claim 7, wherein the scanning side driving circuit (12) includes the staircase wave generating circuits (16 to 19), and a voltage ($V_w$ +

$V_s$), a superposition of a writing voltage ($V_w$) on a staircase wave voltage ($V_s$) is applied in a linear sequence to the scanning side electrodes (Y1 to Ym) in every scanning period.

15. A drive circuit for a capacitative display device having an array of display elements each comprising a dielectric display material disposed between opposed electrodes, wherein control means is provided for effecting display gradation of a said display element by controlling the signals applied to the electrodes so that the amount by which the voltage across said electrodes exceeds the display threshold voltage increases in a stepwise fashion over a period which is predetermined in accordance with the desired display gradation.

90 3 01 01 8 . 9

Fig.1 Prior Art

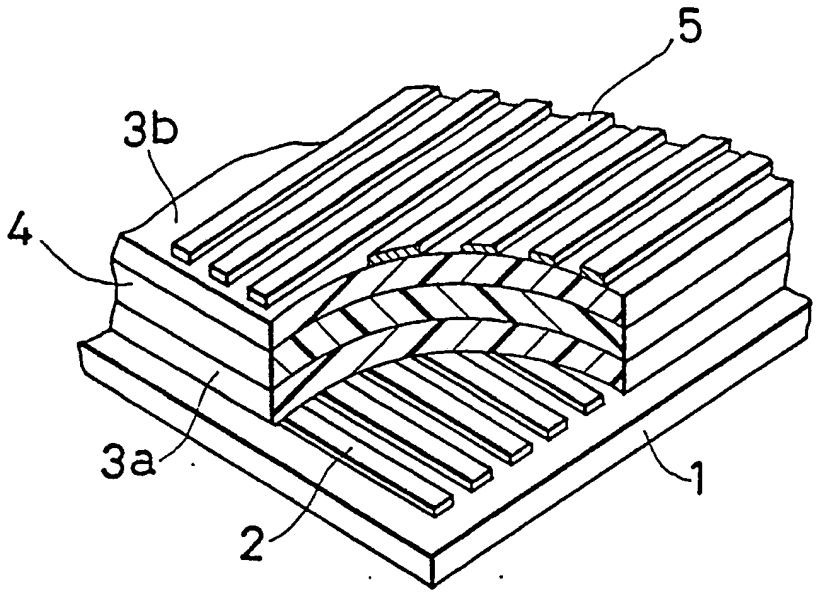



Fig.2 Prior Art

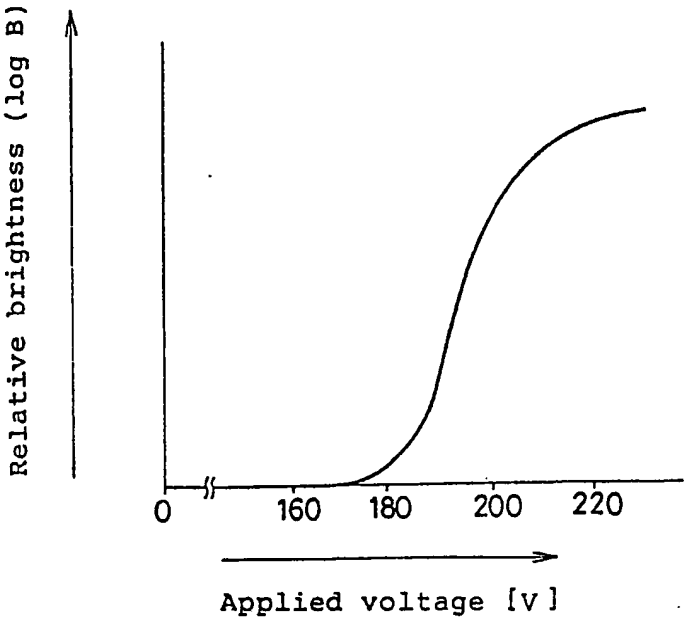


Fig.3 Prior Art

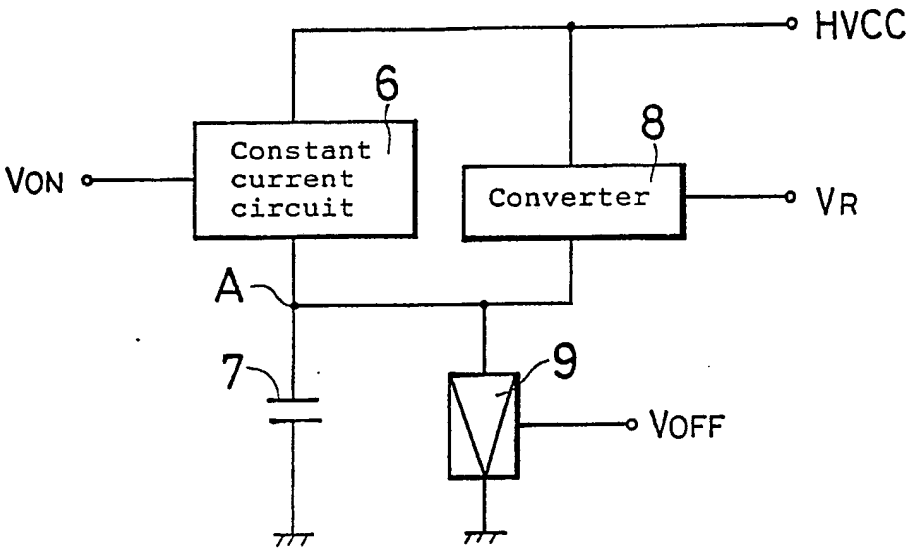



Fig.4 Prior Art

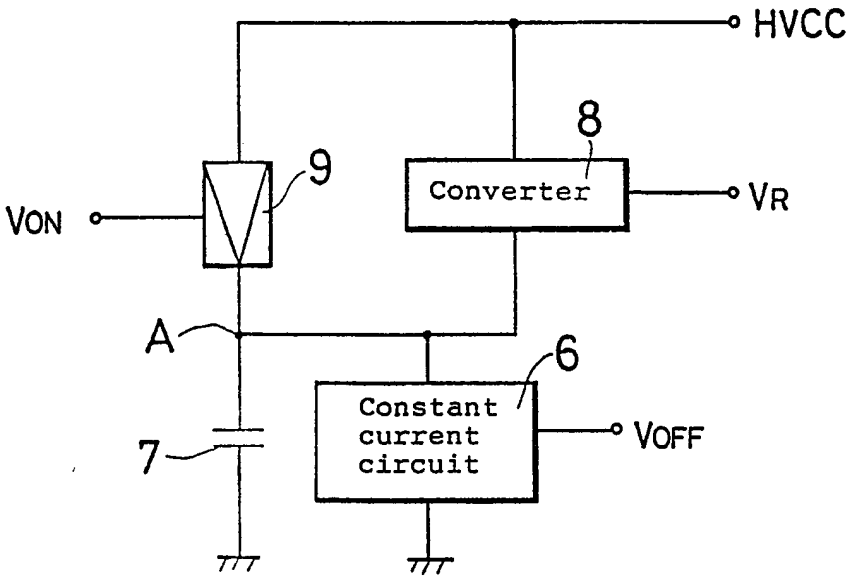


Fig.5(1)Prior Art

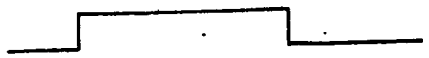



Fig.5(2)Prior Art


Fig.5(3)Prior Art

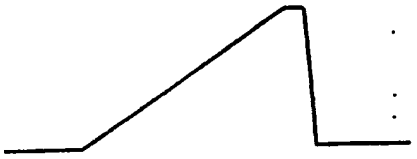



Fig.6(1)Prior Art


Fig.6(2)Prior Art

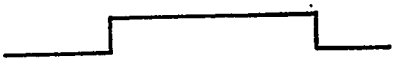



Fig.6(3)Prior Art

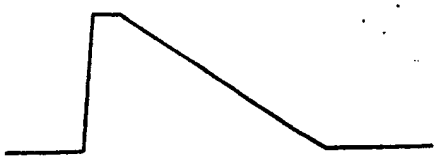


Fig.7

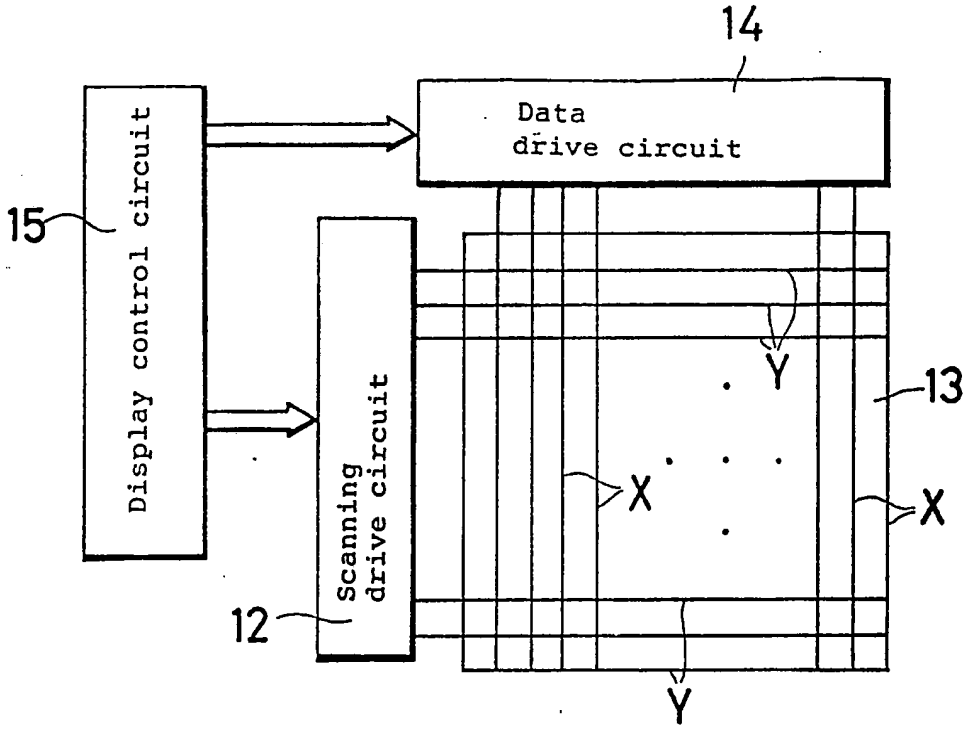

14
Data
drive circuit
15
Display control circuit
Scanning
drive circuit
12
13
Y
X
X
Y

Fig.8

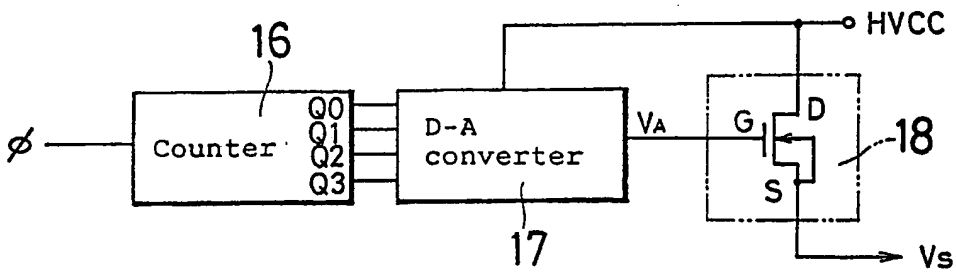

HVCC
16
Counter
Q0
Q1
Q2
Q3
D-A
converter
17
VA
G
D
S
18
Vs

Fig. 9

(1) Clock signal ϕ for gradation

Fig. 9

(2) Counter output

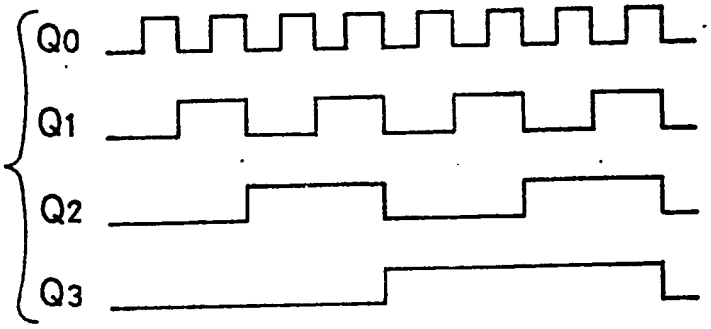



Fig. 9

(3) D-A converter output $V_A$

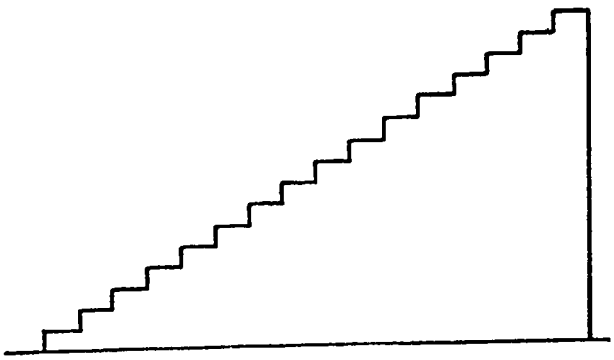
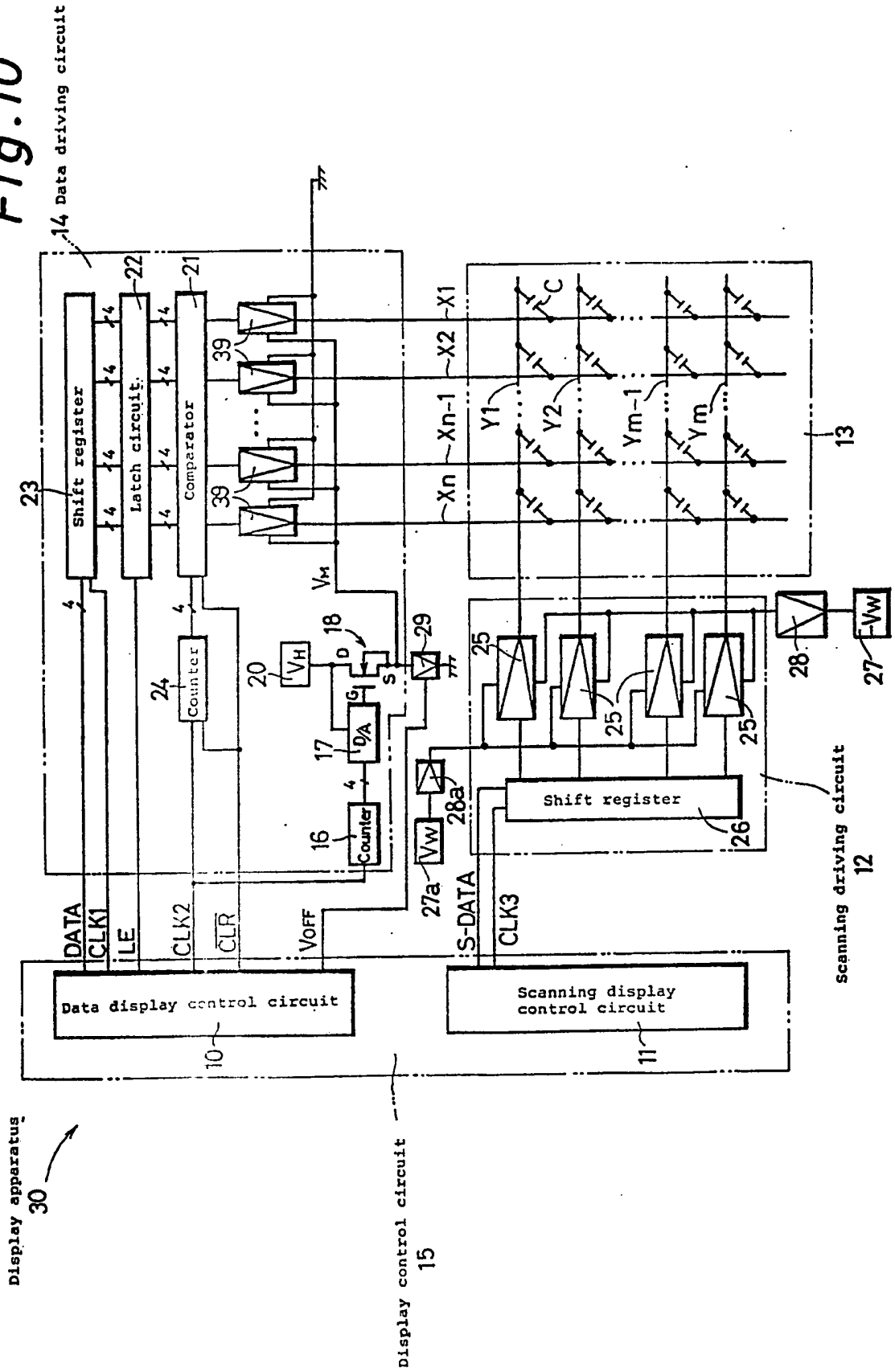


Fig.10


14 Data driving circuit
Shift register
Latch circuit
Comparator
22
21
23
39
X1
X2
Xn-1
Xn
Y1
Y2
Ym-1
Ym
C
13
VH
18
D
S
29
20
24
Counter
17
D/A
16
Counter
28a
27a
VW
28
27
25
26
Shift register
Scanning driving circuit
12
DATA
CLK1
LE
CLK2
CLR
VOFF
S-DATA
CLK3
Data display control circuit
10
Scanning display control circuit
11
Display apparatus
30
Display control circuit
15

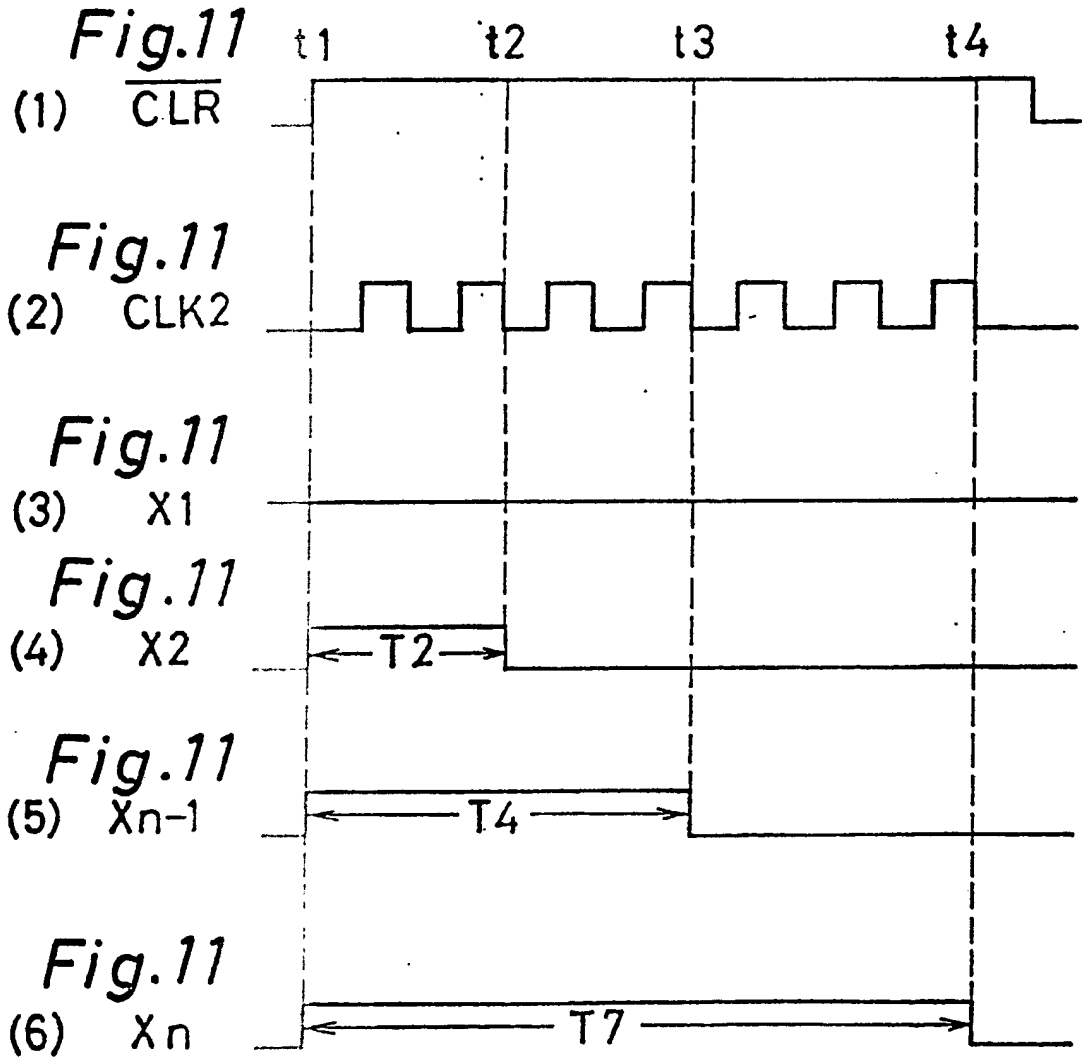


Fig.11
t1
t2
t3
t4
(1) $\overline{CLR}$
Fig.11
(2) CLK2
Fig.11
(3) X1
Fig.11
(4) X2
T2
Fig.11
(5) Xn-1
T4
Fig.11
(6) Xn
T7

Fig. 12

(1) Moduration voltage $V_M$

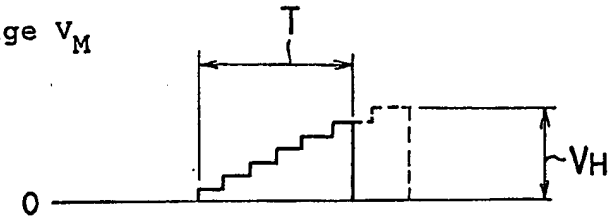



Fig. 12

(2) Writing voltage $-V_W$

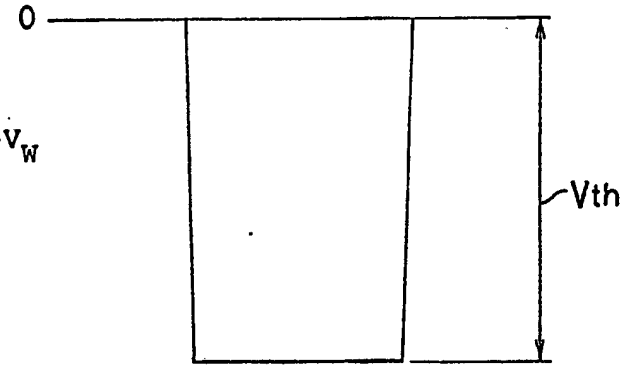



Fig. 12

(3) Driving voltage $V_D$

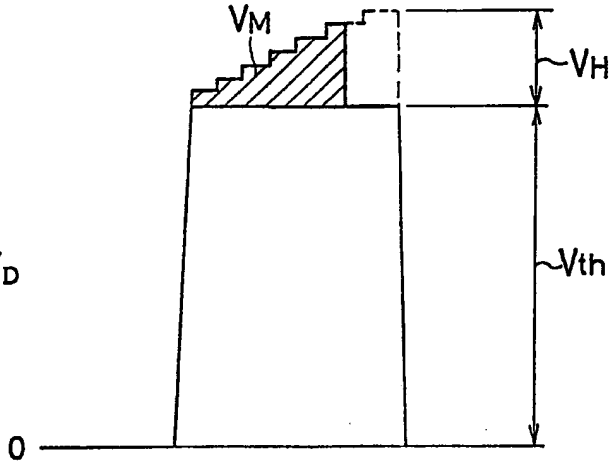


Fig.13
(1)

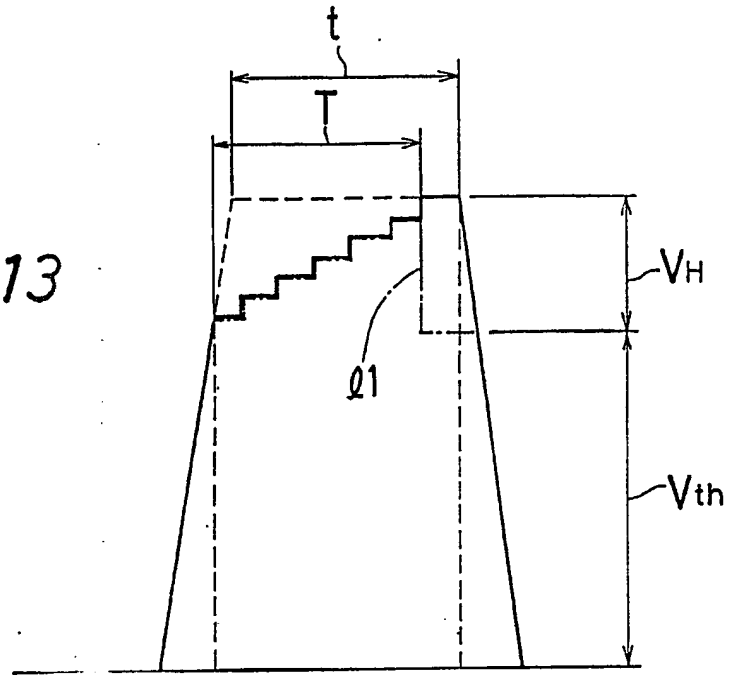



Fig.13
(2)

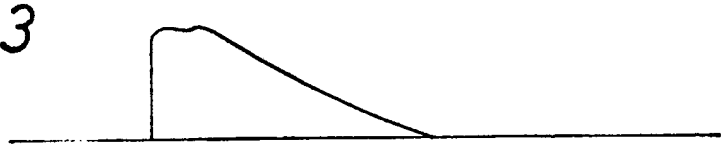


Fig.13
(3)

Fig.14

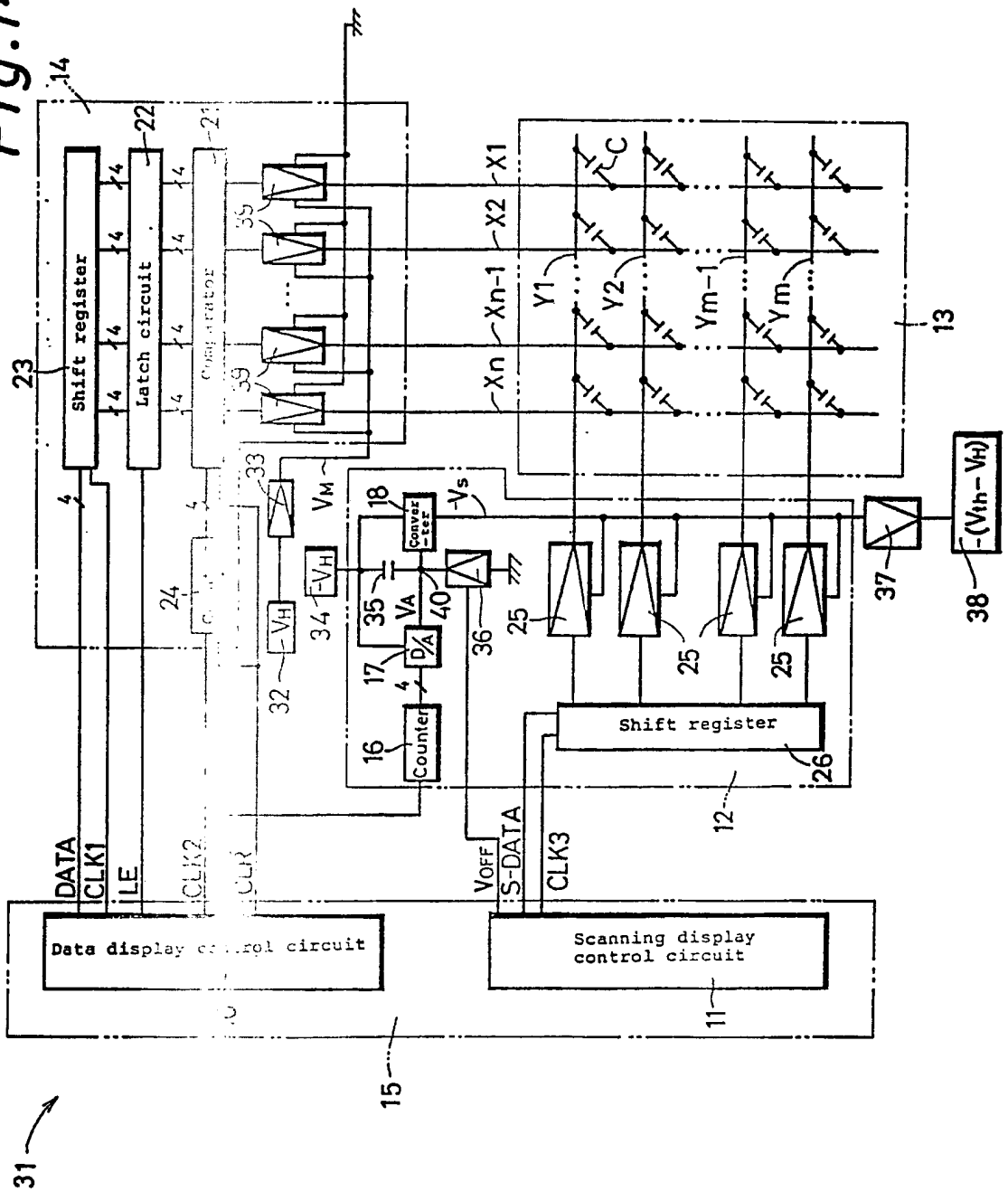

Shift register
Latch circuit
Comparator
Shift register
Counter
Data display control circuit
Scanning display control circuit
DATA
CLK1
ILE
CLK2
CLK
VOFF
S-DATA
CLK3
X1
X2
Xn-1
Xn
Y1
Y2
Ym-1
Ym
C
VM
-VS
-VH
VA
-(Vih-VH)
31
15
11
12
13

Fig 15

(1) Modulation voltage $V_M$

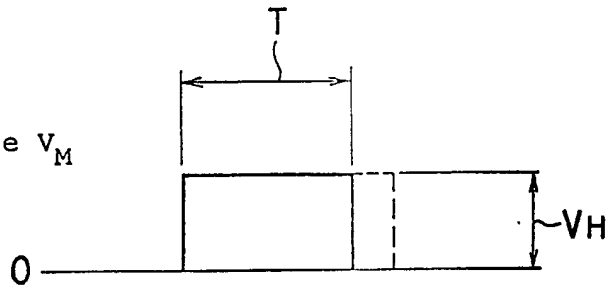



Fig 16

(2) Writing voltage $-V_W$

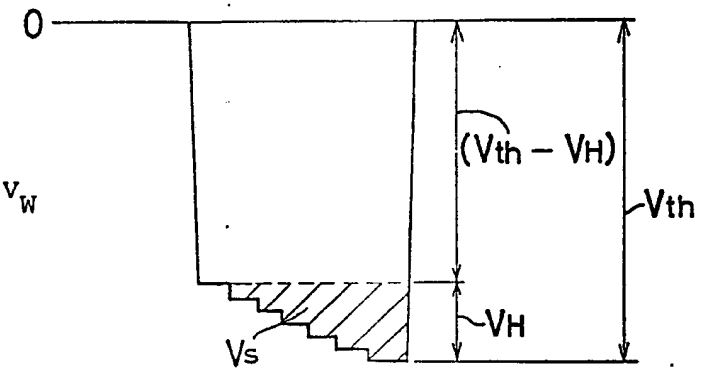



Fig 17

(3) Driving voltage $V_D$

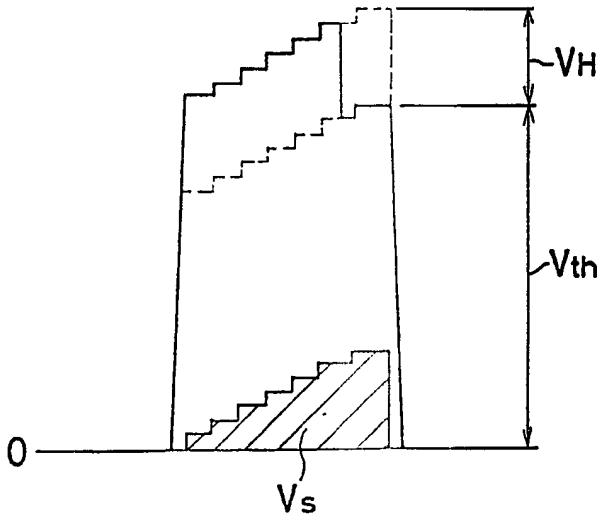


Fig. 16

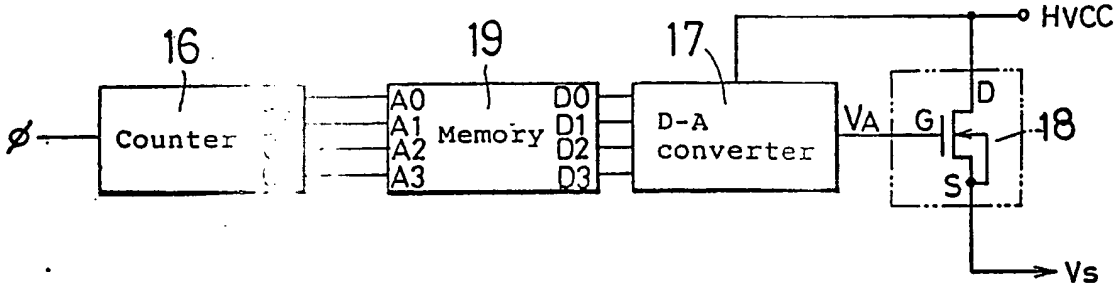



Fig. 17

(1) Clock signal $\phi$ for gradation

(2) Counter output

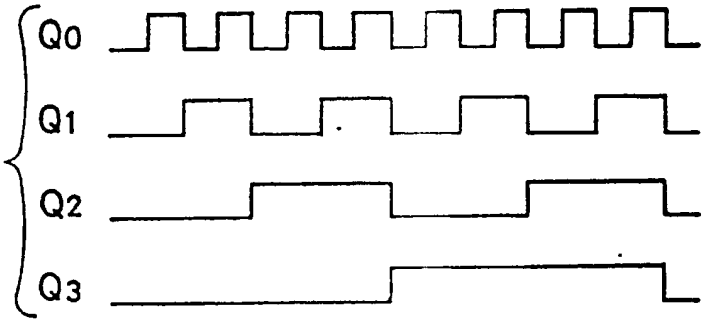
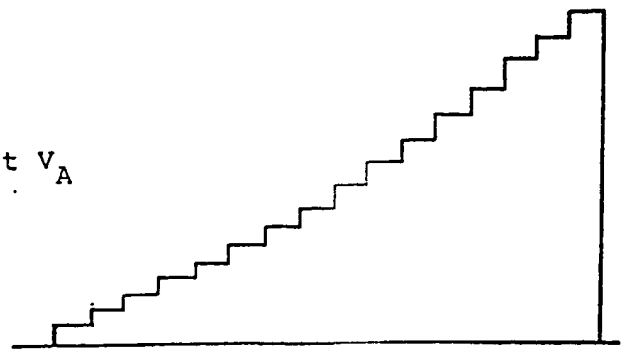



Fig. 18

(3) D-A converter output $V_A$



European Patent Office

# EUROPEAN SEARCH REPORT

Application number

EP 90301018.9

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int Cl⁵) |
|---|---|---|---|
| Y | US - A - 4 353 062 (LORTEIJE) * Abstract; fig. 5 * | 1-8, 14,15 | G 09 G 3/30 |
| A | -- | 9-13 | |
| Y | EP - A1 - 0 016 926 (IBM) * Abstract * | 1-8, 14,15 | |
| A | ---- | 9-13 | |

TECHNICAL FIELDS SEARCHED (Int Cl⁵)

G 09 G 3/00
H 04 N 5/00

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| VIENNA | 30-04-1990 | KUNZE |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1503 03 82